

FPGA Board Support Package

FPGA System Reference Designs and Tools that Give You Complete Control

The Abaco Systems FPGA board support package gives you complete control, flexibility and power to develop solutions for the most demanding DSP applications.

Abaco's Advanced RF and DSP products feature unprecedented configurability. Just as the RF and DSP hardware is designed for maximum adaptability, we built our FPGA board support package (BSP) to maximize flexibility and FPGA resources. We provide the foundational tools for you to fine tune our technology to your specific application.

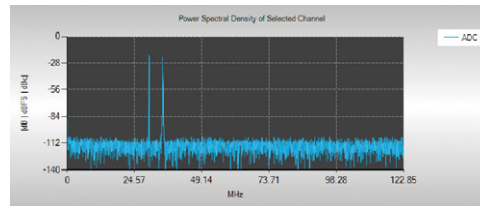
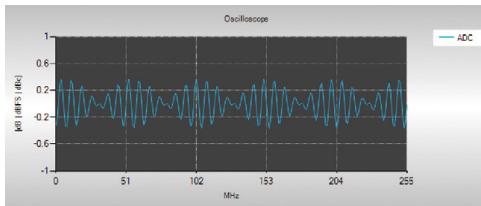
The Abaco FPGA BSP gives you the opportunity to build your specific application requirements on a foundation of pre-validated IP blocks. Our designs minimize FPGA resource utilization and enable you to communicate with onboard peripherals.

Our philosophy with FPGA products is to leave the power with the user by providing completely open FPGA and host reference designs for you to customize and get the full benefit of FPGA-based systems.

At the heart of the Abaco FPGA design methodology is the design flow automation tool – StellarIP. StellarIP is used by Abaco engineers as well as our customers to quickly build FPGA designs for many board configurations.

StellarIP creates a ready to compile FPGA project with complete constraints and synthesis scripts. IP components are built on standard interfaces such as AXI and are reused across different reference designs ensuring reliability.

Board Level Digital and Analog Diagnostics with 4FM GUI and FMC Analyzer



Support across multiple Operating Systems



FEATURES:

Host Tools

- Open source initialization and configuration API Examples.
- Onboard operating system and reference designs for Zynq®-based products
- Support for multiple communication interfaces (Ethernet, PCIe™, etc.)
- Support for Windows®, Linux® and VxWorks®

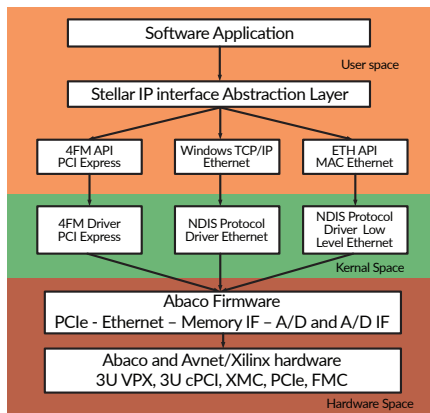
FPGA Tools

- Open source VHDL reference designs to get your hardware up and running quickly
- Prebuilt and tested FPGA reference designs with minimal FPGA resource utilization giving you more resources for your applications.
- Proven design flow methodology with StellarIP
- Critical IP interface cores included (PCIe, JESD204B, DDR, etc.)

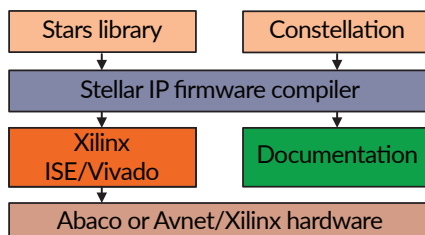
Diagnostic Tools

- Windows GUI for board-level diagnostics
- Board-level interface tests – memory, PCIe, FMC
- Temperature monitoring
- Analog data visualization with FMC analyzer

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Reference Design Layers



Stellar IP design flow

A complete software, firmware and hardware system infrastructure

FPGA-based embedded systems are highly complex since they involve many layers across software, firmware, and hardware. Coordinating communication across these layers can be a daunting engineering task. To help reduce this complexity, Abaco FPGA BSPs are built with a host-centric command architecture with an abstraction layer to hide interface complexities under a communication API.

Onboard FPGA logic is designed as register-level functionality relying on host-coordinated communication for setup and operation. Keeping initialization and configuration intelligence in the software layer frees up powerful FPGA resources for the user to get more out of their FPGA device.

Abaco's BSP provides users with ready to use FPGA and host examples that serve as the backbone of more complex applications. The BSP offers a complete framework that allows command distribution and fast data transfers between a host computer and firmware running in the FPGA. This infrastructure gives users the opportunity to focus on their specific application IP rather than board-level interfaces.

The foundation of the Abaco FPGA reference design is our extensive IP library. Our FPGA reference designs leverage this library and give you the confidence that you are building your application on pre-validated IP.

The IP blocks included in the BSP interface to many digital interfaces such as high speed A/D and D/A interfaces, memory controllers, FIFOs, and scatter/gather PCI Express DMA engines.

With support across several operating systems (Windows 7, Linux and VxWorks) and ready-to-be-used FPGA projects targeting Xilinx® ISE and Vivado, Abaco's board support package embodies a complete design suite for the most advanced projects.

All Abaco cores are coded in VHDL while StellarIP remains language-agnostic. The Xilinx FPGA tools, ISE or Vivado, are supported by StellarIP and projects are automatically created. On the host software side, users can easily access the address space for any of the cores present in the design, thus easily communicating with the hardware.

Custom and application-specific reference designs are possible; contact Abaco Sales to discuss how our hardware and engineering expertise can benefit your application.

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